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10/636,073	08/07/2003	Ronny Lee Arnold	10971189-4	9837

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/636,073	ARNOLD ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-13 and 15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-13 and 15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

Claims 1-3,6-13,15-21 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3,6-8,10,13-20 of U.S. Patent No. 6,643,762 in view of O'Connor (patent No. 6,408,378).

The claims in the instant case are presented side by side with the claims in the claims in the patent 6,643,762 are as follows:

Patent No. 6,643,762	Instant Application
1. A computer system for processing instructions of a computer program, comprising: a plurality of registers;	1. A computer system for processing instructions of a computer program, comprising: a plurality of registers;
a plurality of connection corresponding respectively with said registers;	a plurality of connections corresponding respectively with said registers;
at least one pipeline configured to process and execute said instructions;	at least one pipeline configured to process and execute said instructions;
a scoreboard coupled to said plurality of connections and to said at least one pipeline, said scoreboard having a plurality of bits	a scoreboard coupled to said plurality of connections and to said at least one pipeline, said scoreboard having a plurality of bits

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Corresponding respectively with said plurality of registers, said scoreboard configured to transmit each of said bits across different one of said connections, each of said bits indicative of whether a pending write to a corresponding one of said registers exists;	Corresponding respectively with said plurality of registers, said scoreboard configured to transmit each of said bits across different one of said connections, each of said bits indicative of whether a pending write to a corresponding one of said registers exists;
Decoding circuitry configured to decode at least one encoded register identifier associated with at least one of said instructions into a decoded register identifier, said decoded register identifier having a plurality of bits corresponding respectively with said plurality of registers and identifying at least one of said registers;	Decoding circuitry configured to decode at least one encoded register identifier associated with at least one of said instructions into a decoded register identifier, said decoded register identifier having a plurality of bits corresponding respectively with said plurality of registers and identifying at least one of said registers;
Hazard detection circuitry coupled to each of said plurality of connections said hazard detection circuitry configured to compare each	Hazard detection circuitry coupled to each of said plurality of connections said hazard detection circuitry configured to compare each

Patent 6,643,762	Instant Application
Of said bits decoded register identifier and to detect data hazards based on comparisons of said transmitted bits to said decoded register identifier bits,	Of said bits decoded register identifier and to detect data hazards based on comparisons of said transmitted bits to said decoded register identifier bits,
Wherein said decoding circuitry comprises a decoder configured to receive, from said at least one pipeline, said encoded register identifier and to decode said encoded register identifier into said decoded register identifier, said decoder further configured to transmit said decoded register identifier to said hazard detection circuitry and to said scoreboard.	
2. The system of claim 1, wherein said transmitted bits form a data word transmitted from said scoreboard to said hazard detection circuitry, each asserted bit in said data word indicating that a different one of said registers is	2. The system of claim 1, wherein said transmitted bits form a data word transmitted from said scoreboard to said hazard detection circuitry, each asserted bit in said data word indicating that a different one of said registers is

Patent 6,643,762	Instant Application
Associated with a pending write.	Associated with a pending write.
3. The system of claim 1, wherein said scoreboard includes a plurality of registers, each of said scoreboard registers containing different one of said scoreboard bits and connected to a different one of said one of said connections.	3. The system of claim 1, wherein said scoreboard includes a plurality of registers, each of said scoreboard registers containing different one of said scoreboard bits and connected to a different one of said one of said connections.
4. The system of claim1, wherein said decoded register identifier includes a plurality of bits, wherein each of said bits in said decoded registers identifier that corresponds to a said at least one register is asserted, and wherein the remaining bits in said decoded register identifier are deasserted.	6. The system of claim1, wherein said decoded register identifier includes a plurality of bits, wherein each of said bits in said decoded registers identifier that corresponds to a said at least one register is asserted, and wherein the remaining bits in said decoded register identifier are deasserted.
5. A system for processing instructions of computer programs, comprising:	7. A system for processing instructions of computer programs, comprising:
at least one pipeline;	at least one pipeline;
a plurality of registers;	a plurality of registers;
a plurality of connections,	a plurality of connections,

Patent 6,643,762	Instant Application
Each of said connections corresponding to a different one of said registers;	Each of said connections corresponding to a different one of said registers;
Means for maintaining a plurality of bits and for indicating via said bits which of said registers is associated with a pending write, said maintaining means configured to transmit said bits across said connections, wherein each bit transmitted across each of said connections is indicative of whether the register corresponding to said each connection is associated with a pending write;	Means for maintaining a plurality of bits and for indicating via said bits which of said registers is associated with a pending write, said maintaining means configured to transmit said bits across said connections, wherein each bit transmitted across each of said connections is indicative of whether the register corresponding to said each connection is associated with a pending write;
Hazard detection circuitry configured to perform comparisons between said bits and a decoded register identifier associated with at least one instruction presently in said at least one pipeline, said hazard detection circuitry further configured to detect at least one data hazard based on said comparisons; and	Hazard detection circuitry configured to perform comparisons between said bits and a decoded register identifier associated with at least one instruction presently in said at least one pipeline, said hazard detection circuitry further configured to detect at least one data hazard based on said comparisons.

Patent 6,643,762	Instant Application
Means for receiving for said at least one pipeline an encoded register identifier associated with said at least one instruction and for decoding said encoded register identifier into said decoded register identifier, said decoding means configured to transmit said decoded register identifier to said hazard detection circuitry and to said maintaining mean, said decoded register identifier identifying at least one of said registers.	9. the system of clam 7, further comprising: means for decoding, into said decoded register identifier, an encoded register identifier associated with said at least one instruction, said decoding means configured to transmit said decoded register identifier to said hazard detection circuitry and to said maintaining means, said decoded register identifier identifying at least one of said registers.
6. The system of claim 5, wherein said maintaining means includes a plurality of registers, each of said registers of said maintaining means containing a different one of said bits and connected to a different one of said connections.	8. The system of claim 7, wherein said maintaining means includes a plurality of registers, each of said registers of said maintaining means containing a different one of said bits and connected to a different one of said connections.
7. The system of claim 5, wherein	10. The system of claim 5, wherein

Patent 6,643,762	Instant Application
Said decoded register identifier includes a plurality of bits, wherein each of said bits in said decoded register identifier that corresponds to said at least one register is asserted, and wherein the remaining of said bits in said decoded register identifier are deasserted.	Said decoded register identifier includes a plurality of bits, wherein each of said bits in said decoded register identifier that corresponds to said at least one register is asserted, and wherein the remaining of said bits in said decoded register identifier are deasserted.
8. A method for processing instructions of computer programs, comprising the steps of: processing said instructions via at least one pipeline; providing a plurality of registers; maintaining a plurality of bits within a scoreboard, each of said bits respectively corresponding with one of said registers; providing a plurality of connections each of said connections respectively corresponding with one of said registers; indicating via said bits, which of said registers are associated with pending	13. A method for processing instructions of computer programs, comprising the steps of: processing said instructions via at least one pipeline; providing a plurality of registers; maintaining a plurality of bits within a scoreboard, each of said bits respectively corresponding with one of said registers; providing a plurality of connections each of said connections respectively corresponding with one of said registers; indicating via said bits, which of said registers are associated with pending

Patent 6,643,762	Instant Application
Writes; transmitting, from said scoreboard, each of said bits across a different a different one of said connections; decoding, via decoder, at least one register identifier associated with at least one of said instructions into a decoded register identifier, said decoded register identifier having a plurality of bits corresponding respectively with said plurality of registers and identifying at least one of said registers;	Writes; transmitting, from said scoreboard, each of said bits across a different a different one of said connections; decoding, via decoder, at least one register identifier associated with at least one of said instructions into a decoded register identifier, said decoded register identifier having a plurality of bits corresponding respectively with said plurality of registers and identifying at least one of said registers;
Comparing each of said transmitted bits to a respective one of said bits of said decoded register identifier;	Comparing each of said transmitted bits to a respective one of said bits of said decoded register identifier;
Detecting a data hazard based on said comparing step;	Detecting a data hazard based on said comparing step.
Modifying one of said scoreboard bits scoreboard bits based on said decoded register identifier;	15. method of claim13, further comprising the step of modifying one of said scoreboard bits based one said decoded register identifier.
Transmitting said at least one	

Patent 6,643,762	Instant Application
Register identifier from said at least one pipeline to said decoder; and transmitting said decoded register identifier from said decoder to said scoreboard.	
9. A system for processing instructions of computer programs comprising:	16. A system for processing instructions of computer programs comprising:
a plurality of registers;	a plurality of registers;
a plurality of connections	a plurality of connections
at least one pipeline;	at least one pipeline;
a scoreboard having data indicative of whether each of said plurality of registers is respectively associated with a pending write, said scoreboard configured to transmit said data across said connections;	a scoreboard having data indicative of whether each of said plurality of registers is respectively associated with a pending write, said scoreboard configured to transmit said data across said connections;
hazard detection circuitry coupled to said connections and configured to receive said transmitted data and to perform a comparison between said	hazard detection circuitry coupled to said connections and configured to receive said transmitted data and to perform a comparison between said

Patent 6,643,762	Instant Application
Transmitted data and a decoded register identifier associated with an instruction presently in said at least one pipeline, said hazard detection circuitry further configured to detect a data hazard based on said comparison; **and**	Transmitted data and a decoded register identifier associated with an instruction presently in said at least one pipeline, said hazard detection circuitry further configured to detect a data hazard based on said comparison.
A decoder configured to receive, **from said at least one pipeline,** an encoded register identifier associated with said instruction, said decoder further configured to decode said encoded register identifier and to transmit said decoded register identifier to said hazard detection circuitry and to said scoreboard.	17. A system of claim16, further comprising a decoder configured to receive an encoded register identifier associated with said instruction, said decoder further configured to decode said encoded register identifier into said decoded register identifier and to transmit said decoded register identifier to said hazard detection circuitry and to said scoreboard.
10. The system of claim 9, wherein said transmitted data comprises a plurality of bits, each of said bits indicative of whether a corresponding one of said registers is associated with a	18. The system of claim 17, wherein said transmitted data comprises a plurality of bits, each of said bits indicative of whether a corresponding one of said registers is associated with a

Patent 6,643,762	Instant Application
Pending write.	Pending write.
11.A method for processing instructions of computer programs, comprising the steps of:	19.A method for processing instructions of computer programs, comprising the steps of:
processing said instructions via at least one pipeline;	processing said instructions via at least one pipeline;
using a plurality of registers to execute said instructions;	using a plurality of registers to execute said instructions;
storing, in a scoreboard, data indicative of which of said registers is associated with a pending write;	storing, in a scoreboard, data indicative of which of said registers is associated with a pending write;
transmitting said data from said scoreboard;	transmitting said data from said scoreboard;
decoding, **via a decoder**, an encoded register identifier associated with one of said instructions;	decoding, , an encoded register identifier associated with one of said instructions;
comparing said transmitted data to said decoded register identifier,	comparing said transmitted data to said decoded register identifier; and
detecting a data hazard based on said comparing steps;	detecting a data hazard based on said comparing step.
transmitting said encoded register	21. Method of claim 19,

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Identifier, from said at least one pipeline to said decoder;

Transmitting said decoded register identifier, from said decoder, to said scoreboard; and modifying said data based on said decoded register identifier.

12. The method of claim 11, wherein said transmitted data comprises a plurality of bits, each of said bits indicative of whether a corresponding one of said registers is associated with a pending write.

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comprising the steps of: transmitting said decoded register identifier to said scoreboard and modifying said data based on said decoded register identifier.

20. The method of claim 19, wherein said transmitted data comprises a plurality of bits, each of said bits indicative of whether a corresponding one of said registers is associated with a pending write.

Further comprising modifying one of said bits based on said decoded register identifier.

one of said registers is associated with a pending write.

Patent 6,643,762	Instant Application
11.A method for processing instructions of computer programs, comprising the steps of:	11.A method for processing instructions of computer programs, comprising the steps of:
processing said instructions via at least one pipeline;	processing said instructions via at least one pipeline;
using a plurality of registers to execute said instructions;	maintaining a plurality of bits, each of said bits indicating whether a
storing, in a scoreboard, data indicative of which of said registers is associated with a pending write;	corresponding one of said registers is associated with a pending write;
transmitting said data from said scoreboard;	transmitting a data word including each of said bits, wherein each asserted bit in said data word indicates that a different
decoding, **via a decoder**, an encoded register identifier associated with one of said instructions;	one of said registers is associated with a pending write;
comparing said transmitted data to said decoded register identifier,	receiving said data word;
detecting a data hazard based on said comparing steps;	comparing said data word to a decoded register identifier associated with at
transmitting said encoded register	least one instruction presently in said at least one pipeline; and
	detecting a data hazard based on said comparing step.

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Identifier, from said at least one pipeline to said decoder; Transmitting said decoded register identifier, from said decoder, to said scoreboard; and modifying said data based on said decoded register identifier.	12. The method of claim 11, further comprising the step of modifying one of said bits based one said decoded register identifier.

As can be seen by the side by side layout of the corresponding claims in the instant application and its parent case the claims in each are substantially similar. Claim 1 will be discussed and used a representative claim. The difference in claim 1 which is highlighted in bold indicates that the parent case provided for the transmission of the register identifier data to the scoreboard from the pipeline and from the scoreboard to the pipeline for using preventing data hazards. Claim 1 in the instant application does not particularize this transmission but does specify the use of the data in the scoreboard for preventing hazards and hazard detection circuitry coupled to connections that are connected to the scoreboard. Therefore it would have been obvious to one of ordinary skill in the DP art that in order for the hazards to be determined and prevented the encoded and decoded data for determining hazards would have had to have been transmitted to the pipeline and in response to execution the updated data would have had to have been transmitted to the scoreboard. The other claims in the instant case contain varying scope in the independent claim and where the features not contained in the independent claim of the instant case these features are in the dependent claims but these claims set for the merely an obvious variation to the claims in the parent case as shown above using a side to side comparison.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140

F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tardieux (patent No. 6,810,475) disclosed a processor with pipeline conflict resolution using distributed arbitration and shadow registers (e.g., see abstract).

Bluhm (patent No. 5,630,149) disclosed a pipelined processor with register renaming hardware to accommodate multiple size registers (e.g., see abstract).

Corwin (patent No. 6,550,001) disclosed a system of statistical detection of read after write and write after read hazards (e.g. see abstact).

O'Connor (patent No. 6,408,378) disclosed a multi-bit scoreboarding to handle write after write hazards and eliminate bypass comparators (e.g., see abstract).

Sharahnpani (patent No. 6,272,520) disclosed a method for detecting thread switch events (e.g., see abstract).

Aroroa (patent No. 6,219,781) disclosed a system for performing register hazard detection (e.g., see abstract).Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose

telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER